Active DC Voltage Balancing PWM Technique for High Power 9-Level Cascaded Multilevel Converters

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Abstract— Modulation strategies for multilevel inverters have typically focused on synthesizing a desired set of sinusoidal voltage waveforms using a fixed number of dc voltage sources. This makes the average power drawn from different dc voltage sources unequal and time varying. Therefore, the dc voltage sources are unregulated and require that corrective control action be incorporated. In this paper, first two new selections are proposed for determining the dc voltage sources values for asymmetric cascaded multilevel inverters. Then two modulation strategies are proposed for the dc power balancing of these types of multilevel inverters. Using the charge balance control methods, the power drawn from all of the dc sources are balanced except for the dc source used in the first H-bridge. The proposed control methods are validated by simulation and experimental results on a single-phase 9-level inverter. In this paper, a dedicated pulse width modulation (PWM) technique specifically designed for single-phase (or four wire three-phase) multilevel Cascaded H-Bridge Converters is presented. The aim of the proposed technique is to minimize the DC-Link voltage unbalance, independently from the amplitude of the DC-Link voltage reference, and compensate the switching device voltage drops and on-state resistances. Such compensation can be used to achieve an increase in the waveform quality of the converter. This is particularly useful in high-power low supply voltage applications where a low switching frequency is used. The DC-Link voltage balancing capability of the method removes the requirement for additional control loops to actively balance the DC-Link voltage on each H-Bridge, simplifying the control structure. The proposed modulation technique has been validated through the use of simulation and extensive experimental testing to confirm its effectiveness.

Index Terms—Multilevel converters, predictive control, smart grid.

I. INTRODUCTION

IN Recent years multilevel converters have been identified as a favored topology for high power applications as a result of advantages such as high levels of modularity, availability, overall efficiency, and high output waveform quality. This is achieved at the expense of increased numbers of components and control complexity. In electrical traction drives multilevel inverters have been successfully applied in order to improve system reliability and reduce failures on motor windings as a result of the lower common mode voltages that they produce. The same advantages can be achieved when applied to Hybrid Electric Vehicles. In addition to this functionality, when the dc side is connected to a set of batteries or other energy storage devices the multilevel converter can be used to maintain the charge balance of the energy storage system. Multilevel converters have also been applied for power quality improvement and FACTS where, especially in aerospace applications, the reduced filtering requirement needed for multilevel converter represents an advantage in terms of total converter weight and cost. In the coming years, multilevel converters are likely to be used increasingly in electrical power grids in order to achieve a higher flexibility and reliability and allow smart power management in the presence of different energy sources and utilities connected to the grid. An example is the replacement of distribution level substation transformers with high power multilevel back-to-back converters. In all the aforementioned applications, multilevel converters are being increasingly considered as a fundamental technology, as a result of their capability to handle high-power, utilizing low voltage power devices, while maintaining superior quality output waveforms, even at low device switching frequency. Among all the possible multilevel converter topologies Cascaded H-Bridge converters (CHB) represent an interesting solution in several applications where its reduced number of components when compared to other multilevel converter topologies and high modularity are important features which lend themselves to the improvement of overall system...
efficiency and reliability. Even though three-phase converters are widely used in high power applications, a single-phase configuration is largely employed in Photovoltaic inverters, traction applications or in neutral-connected three-phase power distribution systems. The main issues with the CHB converter is the requirement for isolated DC-Link voltages as well as the significant effect of device voltage drop and on-state resistance in applications with high number of levels and relatively low application ac side voltages. Furthermore, in the active rectifier configuration, balanced DC-Link voltages are required to achieve optimal operation considering a symmetrical (and therefore fully modular) configuration. DC-Link voltage balancing methods have been proposed in literature for CHB active rectifiers and they can be divided into two main groups depending on whether the DC-Link voltage balancing method is integrated in the controller, using additional control loops, or directly into the modulator. In this paper, the latter case is considered and a novel modulation technique, developed for single-phase systems and suitable for high power multilevel CHB converters, is introduced. The proposed modulation strategy is based on the Distributed Commutation Modulator (DCM), described in. DCM is a pulse width modulation (PWM) technique specifically designed for multilevel CHB converters. The aim of DCM is to minimize the commutation frequency of the individual devices, distributing these commutations evenly among the converter HB cells. As a result, the converter losses are equally distributed across the devices, increasing the converter reliability, without compromising the

Fig. 1. (a) Schematic diagram of a 9-level CHB in active rectifier configuration, and (b) a single HB circuit.
demonstrated for a single phase 9-level converter in Section IV, while experimental results from low voltage testing on a laboratory prototype are presented in Section V.

**TABLE I**

**POSSIBLE VOLTAGE LEVELS OF A 4-CELL CONVERTER**

<table>
<thead>
<tr>
<th>H-Bridge states</th>
<th>$V_{com}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>(111)</td>
<td>$+3V_{DC}$</td>
</tr>
<tr>
<td>(110)(011), (101)</td>
<td>$+2V_{DC}$</td>
</tr>
<tr>
<td>(010)(001), (001)</td>
<td>$+V_{DC}$</td>
</tr>
<tr>
<td>(000), (011), (111)</td>
<td>$0V_{DC}$</td>
</tr>
<tr>
<td>(100)(001), (001)</td>
<td>$-V_{DC}$</td>
</tr>
<tr>
<td>(010)(001), (001)</td>
<td>$-2V_{DC}$</td>
</tr>
<tr>
<td>(000), (011), (111)</td>
<td>$-3V_{DC}$</td>
</tr>
</tbody>
</table>

**II. CASCADED H-BRIDGE CONVERTERS**

In Fig. 1 the schematic diagram of a single-phase 7-level CHB converter, connected as an active rectifier, is shown. Although the proposed method is equally as effective in the inverter mode configuration, in order to test the capability of a DC-Link voltage balancing algorithm and avoid the necessity of isolated high voltage sources, the rectifier configuration is preferred. Referring to Fig. 1, the HBs are series-connected on the grid side and an inductive filter $L$, with a parasitic resistance $r_L$, is used to facilitate the required connection between the converter and the grid. Each HB cell is connected to a capacitor, $C$, and a resistor, $R$, used to represent the loading of the converter, which in reality could potentially be another converter, providing back-to-back operation, or a real load. For a symmetrical converter, the generic $i$th cell is connected to a voltage source and can produce three voltage levels, indicated as $-V_{DC}i$, 0 and $+V_{DC}i$. These voltage levels are associated, respectively, to states $-1$, 0 and 1. As a consequence, an $n$-cell cascaded converter can produce $2n + 1$ voltage levels on the ac side. The output voltage $V_{CONV}$ is composed of seven different voltage levels which can be produced by one or more combinations of H-Bridge states, as indicated in Table I.

**III. PROPOSED MODULATION TECHNIQUE**

As stated in the introduction, the main goal of the proposed modulation method is to minimize DC-Link voltage imbalances and compensate the device voltage drops and on state resistances. To achieve such a result, a fast response to any unbalance on the dc loads is required. For this reason the balancing algorithm is fully integrated into the modulation scheme, without using any additional controllers. It is important to note that since one of the targets of the proposed algorithm is to equalize the voltages on the capacitors, their average value is considered as the reference voltage for each DC-link capacitor in the algorithm, while the total DC-Link voltage is set to the reference value using a Proportional-Integral action external to the modulator. In order to reduce stress on the power switches and improve their reliability, the commutations are permitted only between adjacent voltage levels i.e., it is possible to switch only one leg of one H-Bridge cell during every sampling interval. The algorithm is modular and applicable to a generic $n$-level CHB converter; however increasing the number of voltage levels requires an obvious increase in computational effort.

**A. Control**

Fig. 2. shows the control block diagram implemented for the converter of Fig. 1, where $V_{DC}$ denotes the total DC-Link voltage and $V_{DC^*}$ is the desired DC-Link voltage. A single phase Phase-Locked-Loop (PLL) is used in the control scheme to obtain the supply phase angle, $\theta$, and RMS value, $V_s, RMS$. The PLL scheme is obtained by cascading the orthogonal
system generator proposed in, based on the Second Order Generalized Integrator, with the three-phase PLL presented in, based on a steady-state linear Kalman filter. The line current is controlled in order to obtain the required DC-Link voltage; to achieve this goal, the current reference \( I^* \) is calculated, at every sampling period \( T_s \) of the controller, as follows.

\[
I^* (t_k + i T_s) = \frac{P^*}{V_{\text{RMS}} \sqrt{2}} \sin(\theta + iT_s), i = 1, 2 \tag{1}
\]

where \( P^* \) is the required power, imposed by the voltage PI controller and \( t_k \) is the current time instant. The current reference \( I^* \) is predicted at two sampling instants, \( T_s \) and \( 2T_s \), in order to obtain a Dead-Beat current control law, described in for various converter configurations, and in, specifically for the proposed 7-Level CHB. The obtained control law is used to derive the desired voltage reference \( V_{\text{CONV}} \) according to the following expression.

\[
V_{\text{CONV}}(t_k + T_s) = V_d(t_k + T_s) - \frac{L}{2T_s} I^*(t_k + T_s) - I(t_k) + r_L I^*(t_k + T_s). \tag{2}
\]

The control output represents the desired converter voltage average value during the next sampling interval, applied using the proposed modulation scheme.

**B. Distributed Commutation Modulator (DCM)**

As mentioned in the introduction, the proposed technique can be seen as an improvement to the DCM technique, where the commutations are distributed among the three H-Bridges in order to reduce the device switching frequency, and optimize the converter losses. Under normal operating conditions, the \( n \) converter cells are able to commutate sequentially so that each one can perform only one commutation every \( n \) sampling periods. Commutations are permitted only between adjacent voltage levels. As a consequence, the total switching frequency is half of the sampling frequency, while the device switching frequency of a single cell is approximately \( 1/(n - 1) \) for an \( n \)-level CHB. An example of normal operation is given in Fig. 4 where the 9-Level CHB of Fig. 1 is controlled in order to obtain a positive square waveform. As it is possible to see from the first waveform in Fig. 3, given a sampling frequency \( f_s = 1/T_s \), the waveform produced

by the 7 level CHB has a switching frequency \( f_{sw} = f_s \).

The H-Bridges are forced to commutate sequentially obtaining a switching frequency for a single H-Bridge of \( f_{swHB} = f_{sw}/3 \). Taking advantage of the zero vector redundancy, it is possible to obtain, for the device \( Q_1 \) of the H-Bridge 1, a switching frequency equal to \( f_{swQ1} = f_{swHB}/2 \). Clearly this operation condition is not always feasible when a multi-level waveform is produced and the modulation algorithm attempts to distribute the commutations among the devices. Two main issues have been identified using this technique. The DC-Link voltage balance is achieved with a symmetrical load on the three HBs and in any other case an additional control is required. The second issue appears in the case of high-power but relatively low voltage applications utilizing a large number of CHB cells, where the device voltage drops and on-state resistances can negatively affect the behavior of the modulator. An additional algorithm, described below, has been implemented to overcome these issues.

**C. Device Voltage Drop and On-State Resistance Compensation**

The device voltage drop and on-state resistance effect is compensated considering, instead of the measured DC-Link voltages, the effective voltages generated by the converter. For each HB cell, three parasitic voltages, which are dependent on the current direction and amplitude, are defined as

\[
V_o = \text{sign} (I) \times (V_d + V_q) - I \times (R_d + R_q) \tag{3}
\]

\[
V_+ = -2 \times (V_q + |I| R_q) \tag{4}
\]

\[
V_- = 2 \times (V_q + |I|R_d) \tag{5}
\]

In (3)–(5) the actual voltages generated by the converter are calculated on the basis of the diode and transistor voltage drops \((V_d, V_q)\), the diode and transistor on state resistances \((R_d, R_q)\), and on the current \( I \) flowing through the HB. In particular, when
a zero voltage state is applied, the voltage $V_{DC_{eff}}$ produced at the output of the $i$th cell is defined by the following equation:

$$V_{DC_{eff}[i]} = V_0$$  \hspace{1cm} (6)

On the other hand, in case of positive power flowing through the HB cell (applied voltage and ac current have the same sign) the transistor are on and generate the voltage defined by the following equation:

$$V_{DC_{eff}[i]} = V_{DC[i]} + V_+.$$  \hspace{1cm} (7)

Similarly, in case of negative power flow through the HB cell, the transistors are on and generate the voltage defined as follow:

$$V_{DC_{eff}[i]} = V_{DC[i]} + V_-.$$  \hspace{1cm} (8)

**D. DC Link Voltage Balancing Algorithm**

A simplified block diagram of the voltage balancing algorithm is presented in Fig. 4 for a 3-cell converter. The scheme is based on the application of iterative conditions in order to achieve the desired balance of the DC-Link voltages without losing the modularity of the algorithm. The modulation algorithm begins with an update of the actual order of commutation of the 3 H-Bridges. From the measured DC-Link voltages on each capacitor, $V_{DC[1]}$, $V_{DC}$, $V_{DC}$, the average DC-Link voltage $V_{DC_{avg}}$ is calculated as in (9) and considered as a reference value

$$V_{DC_{avg}} = \frac{(V_{DC[1]} + V_{DC[2]} + V_{DC[3]} + V_{DC[4]})}{4}.$$  \hspace{1cm} (9)

Then, the DC-Link voltage error $V_{DC_{err}}$ is calculated for every HB from

$$V_{DC_{err}[i]} = V_{DC_{avg}} - V_{DC[i]}.$$

The switching order for the HBs is determined by the ranking, from the largest to the smallest, of the $V_{DC_{err}}$ absolute values. Supposing that $k$th HB has been selected for the next switching, it is possible to calculate the normalized voltage error $dv$ that has to be compensated by the selected HB as follows:

$$dv = \frac{V^{\ast} - \sum_{i} state(i) \cdot V_{DC_{eff}[i]}}{V_{DC_{eff}[k]}}, state(k) \neq 0$$

$$dv = \frac{V^{\ast} - \sum_{i} state(i) \cdot V_{DC_{eff}[i]}}{V_{DC_{eff}[k]}}, state(k) = 0$$

where $V^{\ast}$ is the voltage reference value and state($i$) the current state of the generic $i$th HB. In other words, $dv$ corresponds to the normalized voltage that the selected $k$th HB has to produce in the next sampling period on the basis of its current voltage level and the subsequent one. Under steady state operation usually $|dv| < 1$; however it is possible, especially during fast transients of the voltage reference, that the absolute value of $dv$ becomes larger than 1. Before performing any commutation, the modulator checks if the selected $k$th HB is able to switch, considering its current state, and how the subsequent commutation will affect the DC-Link voltage balancing. The following three cases, valid for $dv > 0$ and referred to the selected $k$th HB state, are possible.

1) **State($k$) = -1**: the selected HB is not able to generate the required positive voltage with only one commutation, thus the error is reduced applying the 0 voltage level for the whole sampling period. The commutation is permitted only if $V_{DC_{err}[k]}$ and the ac current $I$ have the same sign.

2) **State($k$) = 0**: the selected HB is able to generate the required positive voltage with only one commutation, thus the switching instant is calculated as in (13) or in (14), depending on the ac current sign.

$$t_x = T_m \left[ 1 - \left( \frac{V^{\ast}}{V_{DC[i]}} \right) \right], \quad I \leq 0$$

$$t_x = T_m \left( \frac{V^{\ast}}{V_{DC[i]}} - 1 \right), \quad I > 0$$
\[ t_x = T_m \left[ 1 - \left( dv - \frac{V}{V_{DC}[k]} \right) \right], \quad I \geq 0 \quad (14) \]

If \( dv > 1 \), it is clear from (13) and (14) that \( t_x < 0 \). In this case \( t_x = 0 \) is imposed. The commutation is permitted only if \( V_{DCerr}[k] \) and the ac current \( I \) have the same sign.

3) \textbf{State}(k) = 1: \) the selected HB is not able to not able to generate the required positive voltage. When \( dv < 1 \), the voltage error is reduced by applying the 0 voltage level at the switching instant calculated by (15).

\[ t_x = T_m \left[ 1 - \left( dv - \frac{V_0}{V_{DC}[k]} \right) \right], \quad (15) \]

The commutation is permitted only if \( V_{DCerr}[k] \) and the ac current \( I \) have different signs.

4) \textbf{Otherwise}: \) the modulator checks if another HB is able to switch to a higher voltage level without an increase the DC-Link voltage unbalance.

In case of \( dv < 0 \), the following three cases for the selected \( k \)th HB state are possible.

1) \textbf{State}(k) = 1: \) the selected HB is not able to generate the required negative voltage with only one commutation, thus the error is reduced applying the 0 voltage level for the whole sampling period. The commutation is permitted only if \( V_{DCerr}[k] \) and the ac current \( I \) have different signs.

2) \textbf{State}(k) = 0: \) the selected HB is able to generate the required negative voltage with only one commutation, thus the switching instant is calculated as follows:

\[ t_x = T_m \left[ 1 + \left( dv - \frac{V}{V_{DC}[k]} \right) \right], \quad I \leq 0 \quad (16) \]
\[ t_x = T_m \left[ 1 + \left( dv - \frac{V_0}{V_{DC}[k]} \right) \right], \quad I \geq 0 \quad (17) \]

If \( dv < -1 \), by considering (16) and (17) it is clear that \( t_x < 0 \). In this case \( t_x = 0 \) is imposed. The commutation is permitted only if \( V_{DCerr}[k] \) and the ac current \( I \) have different signs.

3) \textbf{State}(k) = -1: \) the selected HB is not able to generate the required negative voltage. For the case where \( dv > -1 \), the voltage error is reduced applying the 0 voltage level at the switching instant calculated by (18)

\[ t_x = -T_m \left( dv - \frac{V_0}{V_{DC}[k]} \right), \quad (18) \]

The commutation is permitted only if \( V_{DCerr}[k] \) and the ac current \( I \) have the same sign.

4) \textbf{Otherwise}: \) the modulator checks if another HB is able to switch to a higher voltage level without an increase the DC-Link voltage unbalance.

**IV. SIMULATION RESULTS**

Simulations have been carried out in order to compare the performance of the proposed modulation strategy. The power rating of the converter considered in simulation match the power rating used in the experimental tests (3 kW). Operation in rectifier mode has been used to avoid the requirement of isolated high voltage sources. The proposed method, however, is equally as effective in the
inverter mode configuration. A Dead-Beat current control, described in, is used to impose the desired voltage reference. The complete control scheme is shown in Fig. 3 while the simulation parameters are shown in Table II. In order to highlight the effect of parasitic components, large values of $V_d$ and $V_q$ are considered during simulations. In this paper, the proposed modulator is compared with the DCM technique illustrated in . A comparison between the DCM technique and other well-known modulation techniques for CHB converters has already been carried out in . In Fig. 5(a) and 6(a) it is possible to appreciate that the total DC-Link voltage is correctly regulated at the reference value with an optimal DC-Link voltage balance. However, with the proposed modulation strategy the DC-Link voltage oscillations are reduced, when compared to those observed with DCM. In Fig. 5 the line current and the grid voltage are shown for a switching frequency of 1.25 kHz. For the proposed technique the current is correctly regulated with the required phase alignment between grid voltage and current. The proposed modulation strategy also produces a lower total harmonic distortion (THD) value, compared with DCM, due to the active compensation of device voltage drops and on-state resistances which reduces the line current distortion. Fig. 5(e) and 6(e) illustrate, for both techniques, the converter output voltage versus the converter voltage reference and the voltages produced by the single HBs. The commutations are equally distributed among the HBs for both modulation strategies. In order to appreciate the superior capability of the DC-Link voltage balancing of the proposed modulation strategy, three unbalanced dc loads of 10 Ω–20 Ω–30 Ω are implemented in the simulation. Such operating conditions frequently occur in solid state transformers as well as in battery supplied inverters. From Fig. 7(a) and 8(a), which illustrate the DC Link voltages, it is possible to observe that for the proposed modulation strategy the total DC-Link voltage is correctly regulated and the single DC Link voltages are well balanced. When using the DCM technique under the same conditions, an unbalance of the DC-Link voltages is clearly
Simulation results with dc Link voltage balancing algorithm Without DCM for balanced dc loads; DC-Link voltages

Simulation results with dc Link voltage balancing algorithm With DCM for balanced dc loads

Supply Current [I] and Voltage[V]

Converter Voltage

THD analysis

H-Bridge Voltages

Fig: 6(e) H-Bridge Voltages

Fig: 7(a) Voltage[V]

Fig: 7(b) Supply Current [I] and Voltage[V]

Fig: 7(c) THD analysis

Fig: 7(d) Converter Voltage

Fig: 7(e) H-Bridge Voltages

Fig 6. Simulation results with dc Link voltage balancing algorithm With DCM for balanced dc loads

Fig 7. Simulation results with dc Link voltage balancing algorithm Without DCM for unbalanced dc loads
between grid voltage and current. On the contrary, the DCM technique produces a significant distortion on the line current. The proposed modulation strategy clearly generates a lower THD value, compared with DCM. Fig. 6(e) and (f) illustrate, for both techniques, the converter output voltage versus the converter voltage reference as well as the voltages produced by the single HBs. Using the proposed strategy the commutations are not evenly distributed among the HBs anymore. Conversely, using the DCM technique, the even commutation distribution is maintained but the significant harmonic content affects the Dead-Beat controller, producing a distorted voltage reference.

V. CONCLUSION

In this paper, a new modulation concept, suitable for high power low switching frequency cascaded multilevel converters, is introduced. In order to minimize the switching frequency, only one leg of a single H-Bridge cell in each sampling interval is commutated, obtaining a total switching frequency that is the half of the sampling frequency. The aim of the presented modulation technique is to minimize the unbalance of the DC link voltages, for any amplitude of the voltage reference, in order to obtain high quality waveforms while maintaining the modularity of the converter. In order to obtain a quick response to unbalance on the dc loads, the balancing algorithm is fully integrated into the modulation scheme without using any additional controllers. As a consequence, a high bandwidth response for the balancing algorithm is achieved even for extremely unbalanced load conditions. Moreover, device voltage drop and on-state resistance are compensated in order to extend the range of applications of the presented method to those cases where the parasitic effects of the devices may have a considerable effect, as for example automotive applications. The proposed algorithm is verified through simulation and experimental validation. The simulations show that compared to the DCM modulator the proposed modulation technique provides a balance of the DC-Link voltages without compromising the quality of the waveforms, in term of harmonic distortion, with both balanced and unbalanced dc loads. The
modulator also naturally distributes the commutations among the H-Bridge cells in case of balanced dc loads. Experimental tests prove that it is possible to achieve the desired DC-Link voltage balancing even with a variation of 35% of the resistive dc loads. The proposed technique has been tested in comparison with DCM on CHB Back-To-Back converter showing that the proposed effect is not affected by the device parasitic parameters and converter asymmetries. In conclusion, using the proposed technique, it is possible to achieve an optimal balance of DC-link voltages and an active compensation for device parasitic effects in an n-level CHB active rectifier with any configuration of the dc loads, improving the quality of the ac waveforms and maintaining the modularity of the converter. However, clearly, increasing the number of voltage levels would clearly impact the required computational effort and a high-end DSP or microcontroller may be required.

REFERENCES


BIOGRAPHIES

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