IMPROVED TRANSFORMERLESS INVERTER WITH COMMON-MODE LEAKAGE CURRENT ELIMINATION FOR A PHOTOVOLTAIC GRID-CONNECTED POWER SYSTEM

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Abstract—To eliminate the common-mode leakage current in the transformer less photovoltaic grid-connected system, an improved single-phase inverter topology is presented. The improved transformer less inverter can sustain the same low input voltage as the full-bridge inverter of eliminating common-mode leakage current. Both the unipolar sinusoidal pulsewidth modulation (SPWM) as well as the double frequency SPWM control strategy can be applied to implement the three-level output in the presented inverter. The high efficiency and convenient thermal design are achieved thanks to the decoupling of two additional switches connected to the dc side. Moreover, the higher frequency and lower current ripples are obtained by adopting the double-frequency SPWM, and thus the total harmonic distortion of the grid-connected current are reduced greatly. Furthermore, the influence of the phase shift between the output voltage and current, and the influence of the junction capacitances of the power switches are analyzed in detail. Finally, a 1-kW prototype has been simulated and tested to verify the theoretical analysis of this paper.

Index Terms—Common-mode leakage current, junction capacitance, phase shift, photovoltaic (PV) system, sinusoidal pulse width modulation (SPWM) strategy, transformer less inverter.

I. INTRODUCTION

Nowadays, the grid-connected photovoltaic (PV) systems, especially the low-power single-phase systems, call for high efficiency, small size, light weight, and low-cost grid connected inverters. Most of the commercial PV inverters employ either line-frequency or high-frequency isolation transformers. However, line-frequency transformers are large and heavy, making the whole system bulky and hard to install. Topologies with high-frequency transformers commonly include several power stages, which increases the system complexity and reduces the system efficiency. Consequently, the transformer less configuration for PV systems is developed to offer the advantages of high efficiency, high power density, and low cost. Unfortunately, there are some safety issues because a galvanic connection between the grid and the PV array exists in the transformer less systems. A common-mode leakage current flows through the parasitic capacitor between the PV array and the ground once a variable common-mode voltage is generated in transformer less grid-connected inverters. The common-mode leakage current increases the system losses, reduces the grid-connected current quality, induces the severe conducted and radiated electromagnetic interference, and causes personal safety problems.

To avoid the common-mode leakage current, the conventional solution employs the half-bridge inverter or the full-bridge inverter with bipolar sinusoidal pulse width modulation (SPWM), because no variable common-mode voltage is generated. However, the half-bridge inverter requires a high input voltage which is greater than, approximately, 700V for 220-V ac applications. As a result, either large numbers of PV modules in series are involved or a boost dc/dc converter with extremely high-voltage conversion ratio is required as the first power processing stage. The full-bridge inverter just needs half of the input voltage demanded by the half-bridge topology, which is about 350V for 220-V ac applications. But the main drawback is that the full bridge inverter can only employ the bipolar SPWM strategy with two levels, which induces high current ripple, large filter inductor, and low system efficiency. Furthermore, the half-bridge neutral point clamp (NPC) inverter is applied to achieve three or more level output. However, NPC inverter also demands the high input voltage the half-bridge inverter does. Therefore, many advanced inverter topologies for transformer less PV applications were developed such as H5 inverter, HERIC inverter, etc. as shown in Fig. 1.
These topologies need the same low input voltage as the full-bridge inverter and can adopt the unipolar SPWM strategy with three levels. The conclusion drawn from is that various solutions are being researched and employed in transformer less inverters to minimize the common-mode leakage current and improve the efficiency, weight, and size of the whole PV grid-connected power system.

In this paper, an improved grid-connected inverter topology for transformer less PV systems is presented, which can sustain the same low input voltage as the full-bridge inverter and guarantee not to generate the common-mode leakage current. Furthermore, both the unipolar SPWM and the double-frequency SPWM with three-level output can be applied in the presented inverter. The high efficiency and convenient thermal design are achieved by adopting the unipolar SPWM. Moreover, the higher

\[
\nu_{ecm} = \nu_{cm} + \frac{\nu_{dm} L_B - L_A}{2 L_A + L_B}
\]

Fig. 2. Simplified equivalent model of common-mode resonant circuit.

Fig. 1. Advanced inverter topologies for transformer less PV applications. (a) H5 inverter. (b) HERIC inverter. (c) Full-bridge inverter with dc bypass. (d) High-efficiency inverter with H6-type configuration. (e) Karschny inverter. (f) Inverter with two paralleled buck converters.

Equivalent frequency and lower current ripples are obtained by using the double-frequency SPWM. Therefore, a smaller filter inductor can be employed and the harmonic contents and total harmonic distortion (THD) of the output current are reduced greatly, and the grid-connected power quality is improved accordingly.

This paper is organized as follows. The condition of eliminating common-mode leakage current is analyzed in Section II. The improved inverter topology and correlative operation modes under two SPWM control strategies are introduced in Section III. The influence of the power switches’ junction capacitances is illustrated in Section IV. The simulated and experimental results are shown in Section V to explore the performance of the presented inverter. Section VI summarizes the conclusions drawn from the investigation.

II. CONDITION OF ELIMINATING COMMON-MODE LEAKAGE CURRENT

Without an isolated transformer in the PV grid-connected power systems, there is a galvanic connection between the grid and the PV array, which may form a common-mode resonant circuit and induce the common-mode leakage current. The simplified equivalent model of the common-mode resonant circuit has been derived in as shown in Fig. 2, where CPV is the parasitic capacitor, LA and LB are the filter inductors icm is the common-mode leakage current. And, an equivalent common-mode voltage uecm is defined by

\[
u_{ecm} = u_{cm} + \frac{u_{dm} L_B - L_A}{2 L_A + L_B}
\]

Fig. 3. Improved inverter topology
where \( u_{cm} \) is the common-mode voltage, \( u_{dm} \) is the differential-mode voltage, \( u_{AN} \) and \( u_{BN} \) are the output voltages of the inverter relative to the negative terminal N of the dc bus as the common reference.

### III. IMPROVED INVERTER TOPOLOGY AND OPERATION MODES

Fig. 3 shows the improved grid-connected inverter topology, which can meet the condition of eliminating common-mode leakage current. In this topology, two additional switches \( S_5 \) and \( S_6 \) are symmetrically added to the conventional full-bridge inverter, and the unipolar SPWM and double-frequency SPWM strategies with three-level output can be achieved.

#### A. Unipolar SPWM Strategy

Like the full-bridge inverter with unipolar SPWM, the improved inverter has one phase leg including \( S_1 \) and \( S_2 \) operating at the grid frequency, and another phase leg including \( S_3 \) and \( S_4 \) commutating at the switching frequency. Two additional switches \( S_5 \) and \( S_6 \) commute alternately at the grid frequency and the switching frequency to achieve the dc-decoupling states. Accordingly, four operation modes that generate the voltage states of \(+U_{dc}\), \(0\), \(-U_{dc}\) are shown in Fig. 4.

Fig. 5 shows the ideal waveforms of the improved inverter with unipolar SPWM. In the positive half cycle, \( S_1 \) and \( S_6 \) are always ON, \( S_4 \) and \( S_5 \) commute at the switching frequency with the same commutation orders. \( S_2 \) and \( S_3 \), respectively, commute complementarily to \( S_1 \) and \( S_4 \). Accordingly, Mode 1 and Mode 2 continuously rotate to generate \(+U_{dc}\) and zero states and modulate the output voltage. Likewise, in the negative half cycle, Mode 3 and Mode 4 continuously rotate to generate \(-U_{dc}\) and zero states as a result of the symmetrical modulation.

**Mode 1:** when \( S_4 \) and \( S_5 \) are ON, \( u_{AB} = +U_{dc} \) and the inductor current increases through the switches \( S_5 \), \( S_1 \), \( S_4 \), and \( S_6 \). The common-mode voltage is
\[
u_{cm} = \frac{1}{2}(u_{AN} + u_{BN}) = \frac{1}{2}(U_{dc} + 0) = U_{dc}/2
\]

**Mode 2:** when \( S_4 \) and \( S_5 \) are turned OFF, the voltage \( u_{AN} \) falls and \( u_{BN} \) rises until their values are equal, and the anti parallel diode of \( S_3 \) conducts. Therefore, \( u_{AB} = 0V \) and the inductor current decreases through the switch \( S_1 \) and the anti parallel diode of \( S_3 \). The common-mode voltage changes into
\[
u_{cm} = \frac{1}{2}(u_{AN} + u_{BN}) = \frac{1}{2}(0 + U_{dc}) = U_{dc}/2
\]

**Mode 3:** when \( S_3 \) and \( S_6 \) are ON, \( u_{AB} = -U_{dc} \) and the inductor current increases reversely through the switches \( S_5 \), \( S_3 \), \( S_2 \), and \( S_6 \). The common-mode voltage becomes
\[
u_{cm} = \frac{1}{2}(u_{AN} + u_{BN}) = \frac{1}{2}(0 + U_{dc}) = U_{dc}/2
\]

**Mode 4:** when \( S_3 \) and \( S_6 \) are turned OFF, the voltage \( u_{AN} \) rises and \( u_{BN} \) falls until their values are equal, and the anti parallel diode of \( S_4 \) conducts. Similar as to **Mode 2**, \( u_{AB} = 0V \) and the inductor current decreases through the switch \( S_2 \) and the anti parallel diode of \( S_4 \). The common-mode voltage \( u_{cm} \) also keeps \( U_{dc}/2 \) referring to (9).

From (8) to (10), the common-mode voltage can remain a constant \( U_{dc}/2 \) during the four commutation modes in the improved inverter with unipolar SPWM. The switching voltages of all commutating switches are half of the input voltage \( U_{dc}/2 \), and thus, the switching losses are reduced compared with the full bridge inverter. Furthermore, in a grid period, the energies of the switching losses are distributed averagely to the four switches \( S_3 \), \( S_4 \), \( S_5 \), and \( S_6 \) with high-frequency commutations, and it benefits the thermal design of printed circuit board and the life of the switching components compared with H5 inverter.
Fig. 5. Ideal waveforms of the improved inverter with unipolar SPWM.

B. Double-Frequency SPWM Strategy

The improved inverter can also operate with the double frequency SPWM strategy to achieve a lower ripple and higher frequency of the output current. In this situation, both phase legs of the inverter are, respectively, modulated with 180° opposed reference waveforms and the switches S1–S4 all acting at the switching frequency. Two additional switches S5 and S6 also commutate at the switching frequency cooperating with the commutation orders of two phase legs. Accordingly, there are six operation modes to continuously rotate with double frequency and generate +Udc and zero states or −Udc and zero states, as shown in Figs. 4 and 6.

Fig. 7 shows the ideal waveforms of the improved inverter with double-frequency SPWM. In the positive half cycle, S6 and S1 have the same commutation orders, and S5 and S4 have the same orders. S2 and S3, respectively, commutate complementarily to S1 and S4. Accordingly, Mode 1, Mode 2, and Mode 5 continuously rotate to generate +Udc and zero states and modulate the output voltage with double frequency. In the negative half cycle, Mode 3, Mode 4 and Mode 6 continuously rotate to generate −Udc and zero states with double frequency due to the completely symmetrical modulation.

Mode 5: when S1 and S6 are turned OFF, the voltage uAN falls and uBN rises until their values are equal, and the anti parallel diode of S2 conducts.

Therefore, uAB = 0V and the inductor current decreases through the switch S4 and the anti parallel diode of S2. The common-mode voltage ucm keeps a constant Udc/2 referring to (9).

Mode 6: similarly, when S2 and S5 are turned OFF, the voltage uAN rises and uBN falls until their values are equal, and the anti parallel diode of S1 conducts. Therefore uAB = 0V and the inductor current decreases through the switch S3 and the anti parallel diode of S1. The common-mode voltage ucm still is a constant Udc/2 referring to (9).

Under the double-frequency SPWM strategy, the common mode voltage can keep a constant Udc/2 in the whole switching process of six operation modes. Furthermore, the higher frequency and lower current ripples are achieved, and thus, the higher quality and lower THD of the grid-connected current are obtained, or a smaller filter inductor can be employed and the copper losses and core losses are reduced.
Fig. 7. Ideal waveforms of the improved inverter with double-frequency SPWM.

Fig. 8. Two additional operation modes when voltage and current are in different directions. (a) Mode 7. (b) Mode 8.

C. Phase Shift between Output Voltage and Current

There is actually a phase shift between the output voltage $u_{AB}$ and output current $i_g$ in the grid-connected inverter due to the existence of the filter inductance. Two additional operation modes occur in the small regions where the output voltage and current are in different directions, as shown in Fig. 8.

Fig. 9 shows the practical waveforms of the improved inverter when considering the phase shift, where $u_{AB1}$ is the fundamental component of the output voltage $u_{AB}$. In Region I and Region II, the detailed operation principle and modes of the unipolar SPWM and double-frequency SPWM have been analyzed earlier, under the condition that the output voltage and current are in the same direction.

In Region III, the output current is positive. Meanwhile, the output voltage is negative and modulated according to the operation principle in the negative half cycle. Therefore, if the unipolar SPWM strategy is adopted, accordingly Mode 7 and Mode 5 continuously rotate to generate $-U_{dc}$ and zero states. If the double-frequency SPWM strategy is used, Mode 7, Mode 2, and Mode 5 continuously rotate to generate $-U_{dc}$ and zero states with double frequency.

Symmetrically in Region IV, the output current becomes negative, and the output voltage is modulated according to the operation principle in the positive half cycle. Hereby, Mode 8 and Mode 6 continuously rotate to generate $+U_{dc}$ and zero states when the unipolar SPWM strategy is used. Mode 8, Mode 4, and Mode 6 continuously rotate to generate $+U_{dc}$ and zero states with double frequency when the double-frequency SPWM is adopted. With Mode 7, although the switches $S2$, $S5$, $S3$, and $S6$ are ON, and $S1$ and $S4$ are OFF, the positive inductor current only freewheels through the antiparallel diodes $S3$, $S5$, $S6$, and $S2$, and decreases rapidly for enduring the reverse voltage. The common-mode voltage $u_{cm}$ keeps $U_{dc}/2$ referring to (10).

With Mode 8, similarly, the negative inductor current only freewheels through the antiparallel diodes of $S1$, $S5$, $S6$, and $S4$, and decreases rapidly for enduring the reverse voltage.

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<td>Mode 1, Mode 3</td>
<td>4 Switches</td>
<td>$-U_{dc}$</td>
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<tr>
<td>Mode 2, Mode 4, Mode 3, Mode 6</td>
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<tr>
<td>Mode 7, Mode 8</td>
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IV. INFLUENCE OF SWITCHES’ JUNCTION CAPACITANCES

The aforementioned eight operation modes can be classified into two categories based on whether the dc and ac sides of the improved inverter are decoupled.

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not affected by the junction capacitances of any switches.

However, in the dc-decoupling states, Mode 2, Mode 4, Mode 5, and Mode 6, the dc and ac sides are decoupled by turning OFF the additional switch S5 or S6. It becomes more complicated to achieve the condition of eliminating common mode leakage current if considering the junction capacitances of the switches. Actually, when the improved inverter commutates from one of the no decoupling modes to one of the dc-decoupling modes, the slopes of voltage uAN and uBN are determined by the junction capacitances of the switches, and accordingly, the common-mode voltage ucm is affected.

Taking the commutation from Mode 1 to Mode 2 as an example, there are always two stages whether the unipolar SPWM or the double-frequency SPWM strategy is adopted. Other commutations are similar due to the symmetry of the operation modes. Stage I: Fig. 10 shows the transient circuit of the commutation from Mode 1 to Mode 2, where C1–C6 represent the junction capacitors of the switches S1–S6. As shown in Fig. 10(a), when S4 and S5 are turned OFF and the anti paralleled diode of S3 has not conducted to freewheel, three charging or discharging circuits are composed of the junction capacitors C2, C3, C4, and C5. According to Kirchhoff’s current law, the following current equations can be given

\[ C_4 = C_2 + C_5 \]
\[ C_3 = C_1 + C_6 \]

V. SIMULATED RESULTS

In conclusion, there are four commutations from one of the no decoupling modes to one of the dc-decoupling modes, and the following equations can be analyzed and summarized similarly to reach \( u_{AN} = u_{BN} = U_{dc}/2 \) at the end of the transient process in Stage 1, when the unipolar SPWM is adopted.

1) Commutation from Mode 1 to Mode 2: \( C_4 = C_2 + C_5 \).
2) Commutation from Mode 3 to Mode 4: \( C_3 = C_1 + C_6 \).
3) Commutation from Mode 7 to Mode 5: \( C_3 = C_1 + C_6 \).
4) Commutating from Mode 8 to Mode 6: \( C_4 = C_2 + C_5 \).

Therefore, to meet the condition of eliminating common mode leakage current, the value principle of the junction capacitors under the unipolar SPWM is concluded that \( C_4 = C_2 + C_5 \) and \( C_3 = C_1 + C_6 \). (15)

Furthermore, when the double-frequency SPWM is adopted, four additional equations must be added to balance the junction capacitances of the switches.

1) Commutation from Mode 1 to Mode 2: \( C_1 = C_3 + C_6 \).
2) Commutation from Mode 3 to Mode 4: \( C_2 = C_4 + C_5 \).
3) Commutation from Mode 7 to Mode 5: \( C_2 = C_4 + C_5 \).
4) Commutating from Mode 8 to Mode 6: \( C_1 = C_3 + C_6 \).

Similarly, the value principle of the junction capacitors under the double frequency SPWM is concluded that \( C_5 = C_6 = 0, C_2 = C_4 \), and \( C_1 = C_3 \). Considering that the junction capacitance of the switch cannot be zero, the theoretic value principle is modified as next for practical applications: \( C_5 = C_2 = C_4 \) and \( C_6 = C_1 = C_3 \).
Fig. 12. Simulated results by employing the unipolar SPWM when junction capacitances of six switches are equal. Simulated waveforms of $u_{AN}$, $u_{BN}$, and $u_{cm}$.

Fig. 13. Simulated results by employing the unipolar SPWM when two additional capacitors with values of 29 pF are, respectively, paralleled to $S_3$ and $S_4$. (a) Simulated waveforms of $u_{AB}$, $i_g$, and $i_{cm}$. (b) Simulated waveforms of $u_{grid}$ and $i_g$. (c) Simulated waveforms of $u_{AN}$, $u_{BN}$, and $u_{cm}$.
In order to verify the theoretical analysis in previous sections, a 1-kWp PV array is simulated, having the frame of the panels connected to ground with the parasitic capacitance of 75 nF. A 1-kW inverter prototype is also built. The detailed components and parameters used are as follows: output power, $P_{out} = 1$ kW; input voltage, $U_{dc} = 380$ V; input capacitor, $C_{dc}$: 940 $\mu$F; grid voltage, $U_g = 220$ Vac; grid frequency, $f_g = 50$ Hz; switch frequency, $f_s = 20$ kHz; filter inductor, $L_f = 4$ mH; parasitic capacitor, $C_{PV} = 75$ nF; power switches, $S_1$–$S_6$ = junction capacitors of the switches, $C_1$–$C_6$ = 29 pF.

Fig. 12 shows the simulated and experimental results by employing the unipolar SPWM when the junction capacitances of six switches are equal. Since the value principle of the junction capacitors described in (15) is not reached, the relatively large oscillations of the voltages $u_{AN}$, $u_{BN}$, and $u_{cm}$ are induced. As shown in Fig. 12(a), the simulated waveforms indicate that $u_{AN} = u_{BN} = 253$ V at the end point of the transient process from Mode 1 to Mode 2, according to the theoretical analysis in (14). Subsequently, $u_{AN}$, $u_{BN}$, and $u_{cm}$ begin to resonate with the amplitude up to 180 V. The experimental waveforms are shown in Fig. 12(b), which is similar to the simulation, but the resonant amplitude is slightly damped due to the internal resistance of the practical inverter prototype.

Therefore, to accord with the value principle of the junction capacitors under the unipolar SPWM, two additional capacitors with the values of 29 pF are, respectively, paralleled to $S_3$ and $S_4$. Fig. 13 shows the simulated and experimental results. The simulated and experimental waveforms of the grid-connected current $i_g$ are shown in Fig. 13(a) and (b). It is clear that the grid-connected current is highly sinusoidal synchronized with the grid voltage by achieving the three-level output. The experimental THD counted to 50th of the grid-connected current is 2.543%. Furthermore, the simulated waveforms shown in Fig. 13(a) and (d) indicate that when the common-mode voltage $u_{cm}$ keeps 190 V constantly, the common-mode leakage current $i_{cm}$ is almost zero since $u_{AN}$ and $u_{BN}$ are fully complementary in the switching periods. Accordingly, as shown in Fig. 13(c) and (e), in the experimental waveforms, even though the junction capacitances of practical switches are nonlinear and hard to
Fig. 15. Measured efficiency of the improved inverter

Fig. 15 and Table show the detailed efficiency data of the improved inverter including the maximum efficiency and European efficiency, which are measured by the power analyzer PZ4000 from Yokogawa, respectively, when the unipolar SPWM and the double-frequency SPWM are adopted. The maximum efficiency of 97.1% and European efficiency of 95.9% are achieved under the unipolar SPWM. And the maximum efficiency and European efficiency are 96.6% and 95.5% under the double frequency SPWM due to the slight increase of the switching losses.

IX. CONCLUSION

This paper presented an improved grid-connected inverter topology for transformer less PV systems. The unipolar SPWM and double-frequency SPWM control strategies are both implemented with three-level output in the presented inverter, which can guarantee not to generate the common-mode leakage current because the condition of eliminating common-mode leakage current is met completely. Furthermore, the switching voltages of all commutating switches are half of the input dc voltage and the switching losses are reduced greatly. The high efficiency and convenient thermal design are achieved thanks to the decoupling of two additional switches $S_5$ and $S_6$. Moreover, by adopting the double-frequency SPWM, the higher frequency and lower current ripples are achieved. Consequently, the higher quality and lower THD of the grid-connected current are obtained, or the smaller filter inductors are employed and the copper losses and core losses are reduced accordingly. Finally, a 1-kW prototype was built, and the validity and applicability of the improved inverter were confirmed by the simulated results.

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